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The Fu Foundation School of Engineering and Applied Science

ELEN E3106/4106 Lecture 21

MOSFETs Part I

Outline

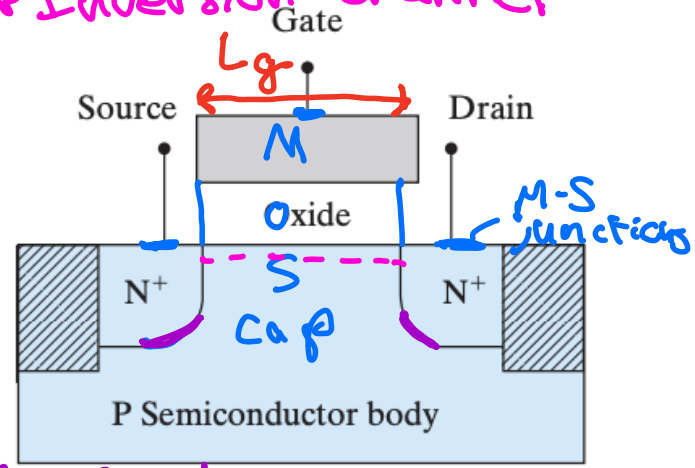
- MOSFET structure
- MOSFET as a switch
- Regions of operation
- Output and transfer characteristics
- CMOS device and circuit technology

Assignments:
Homework 8 due Monday, December 1st by 11:59pm

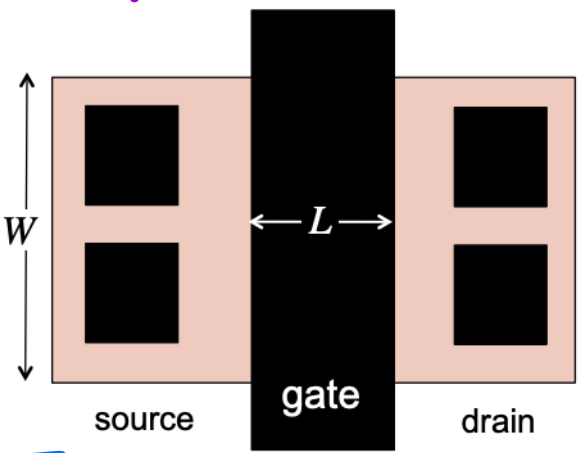
Basic Device Structure

- **M**etal **O**xide **S**emiconductor Field-effect Transistors
- Most prevalent semiconductor device in ICs!
- Essentially, a MOS capacitor with carrier wells on either side. This means we have 2 p-n junctions!
- 3 terminal device
- What is a field-effect transistor (FET)?
  - The voltage on one terminal (gate) creates an E-field through the oxide that either allows or prevents conduction (e.g. current) between the other two terminals (source and drain)
- Unipolar: only one type of charge carrier is significant to their operation unlike BJTs

* Inversion channel



p-n junctions!



Top view

Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*, M. Lundstrom ECE 305 Slides

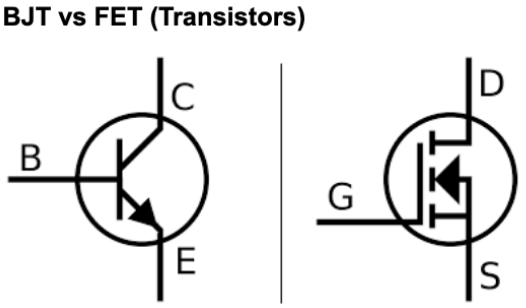
Comparison with BJT and Nomenclature

1. Transistor Amplification: a small signal (I or V, terminal #2) can control a large signal (usually I, flowing between terminal #1 and #3)

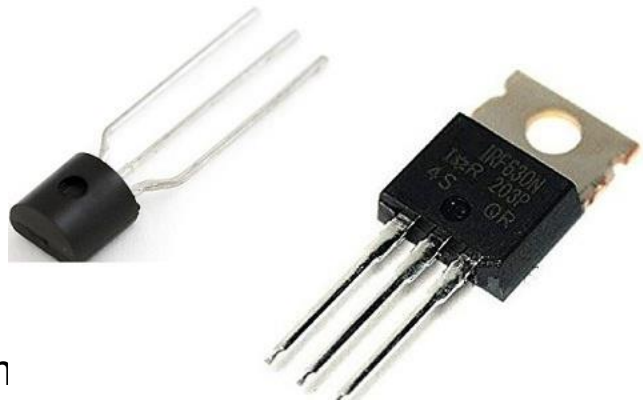
2. Transistor Switching: the transistor can be turned on/off.

1) BJT: small input current (faucet) controls large output current (hose)
e.g. current-controlled current source

2) FET: small input voltage (faucet) controls large output current (hose)
e.g. voltage-controlled current source



- Recall: A terminal is any externally available point of connection (M-S junc., infinite carrier source/sink)
- How many terminals does a transistor **usually** have? 3
  - Terminal 1: brings current into the transistor.
    - BJT: Emitter = MOSFET: source
  - Terminal 2: carriers current out.
    - BJT: Collector = MOSFET: drain
  - Terminal 3: acts as a handle to control the current flow (input term
    - BJT: Base = MOSFET: gate



Sources: Learning about Electronics, EIProCus

Transistor as a "Black Box"

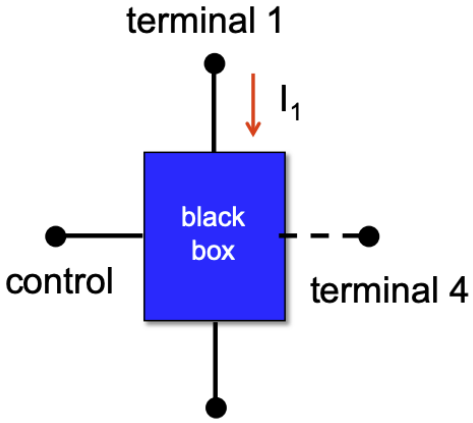
- A black box is any complicated electronic device like a transistor whose behavior can be observed entirely in terms of inputs/outputs even if the internal structure is not known
  - We have already looks at one example: 2-port network
- There are many kinds of transistors!
  - MOSFETs
  - Schottky-barrier (SB) FET
  - High electron mobility transistor (HEMT)
  - FinFET
  - BJT
  - Heterojunction bipolar transistor
  - SpinFET, etc.
  - ....

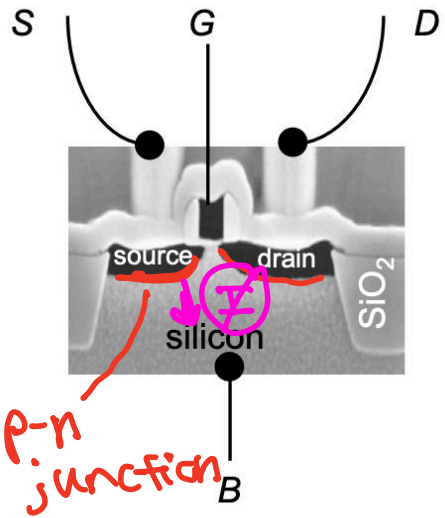
* If interested, take 6333

- What's the 4th terminal for on the diagram on the right?

  Body (semiconductor bulk)

- The body is frequently connected to the source to ensure both p-n junctions at source/body and drain/body are not FB to prevent large unwanted current flowing from body into source or drain



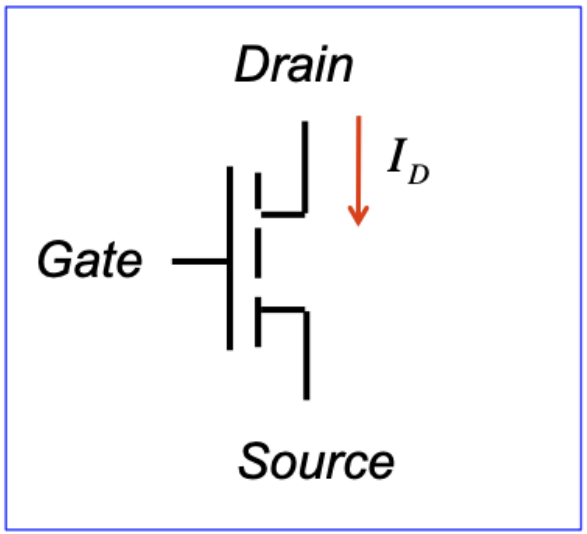


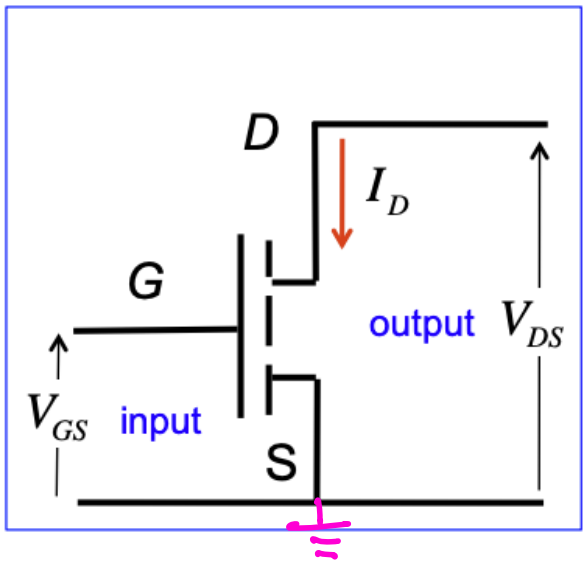
(Texas Instruments, ~ 2000)

Sources: M. Lundstrom ECE 305 Slides

MOSFET Circuit Symbol and Configuration

- Circuit symbol (left) and common source configuration (right). Source is often grounded
- We are interested in the $I - V$ characteristics in terms of the drain current Id, and various voltages
- $I_D - V_{GS}$ for fixed V_{DS} are called the *transfer characteristics*
- $I_D - V_{DS}$ for fixed V_{GS} are called the *output characteristics*





Sources: M. Lundstrom ECE 305 Slides

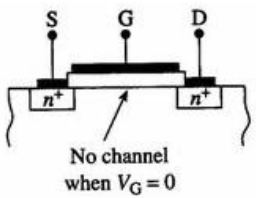
MOSFET Enhancement and Depletion Modes

Two "modes" or types of transistors exist

1. Enhancement-mode ("normally-off"): The channel is devoid of carriers at $V_g = 0\ V$ and $|V_g| > |V_{th}|$ is required to create the channel and turn it "on"
2. Depletion-mode ("normally-on"): The channel is already present and conducts at $V_g = 0\ V$. Device requires an applied V_g to turn it "off"

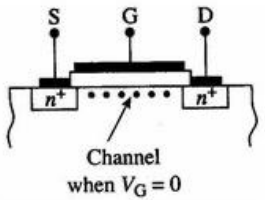
- Modern Si MOSFETs are all enhancement-mode for easier circuit design and better power efficiency, so we will be focusing on e-mode

Enhancement Mode



Conduction between source and drain regions is *enhanced* by applying a gate voltage

Depletion Mode

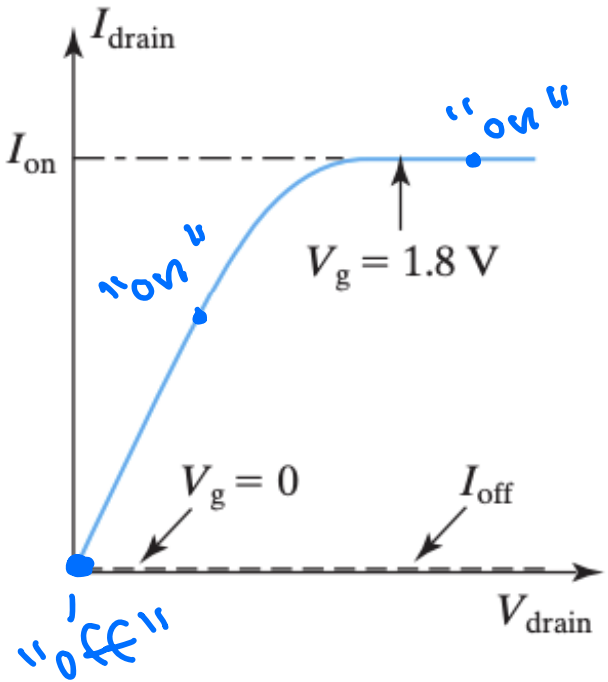


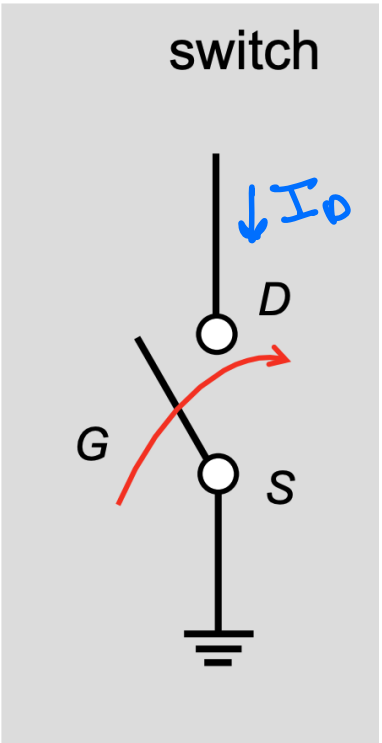
A gate voltage must be applied to *deplete* the channel region in order to turn off the transistor

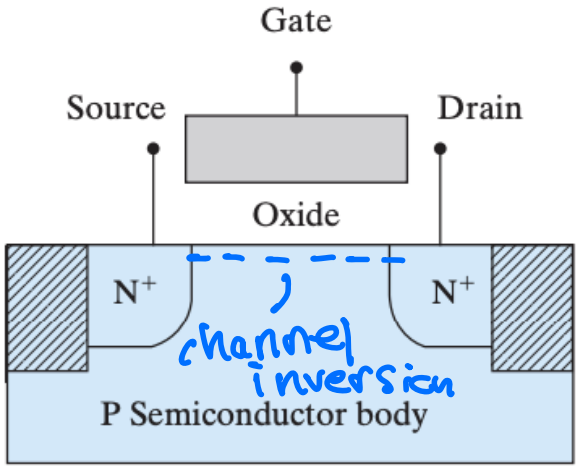
Sources: Quora

MOSFET As a Switch

- At the basic level, we can think of the MOSFET as an on-off switch
- The gate voltage V_G determines whether current I_D flows between the source and drain





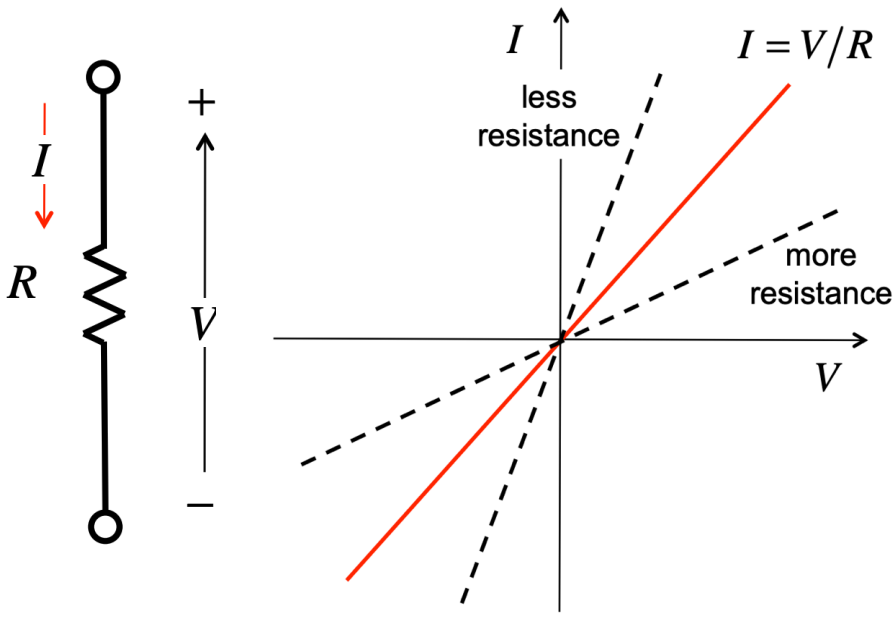


Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*, M. Lundstrom ECE 305 Slides

I-V Characteristics of Basic Two Terminal Components

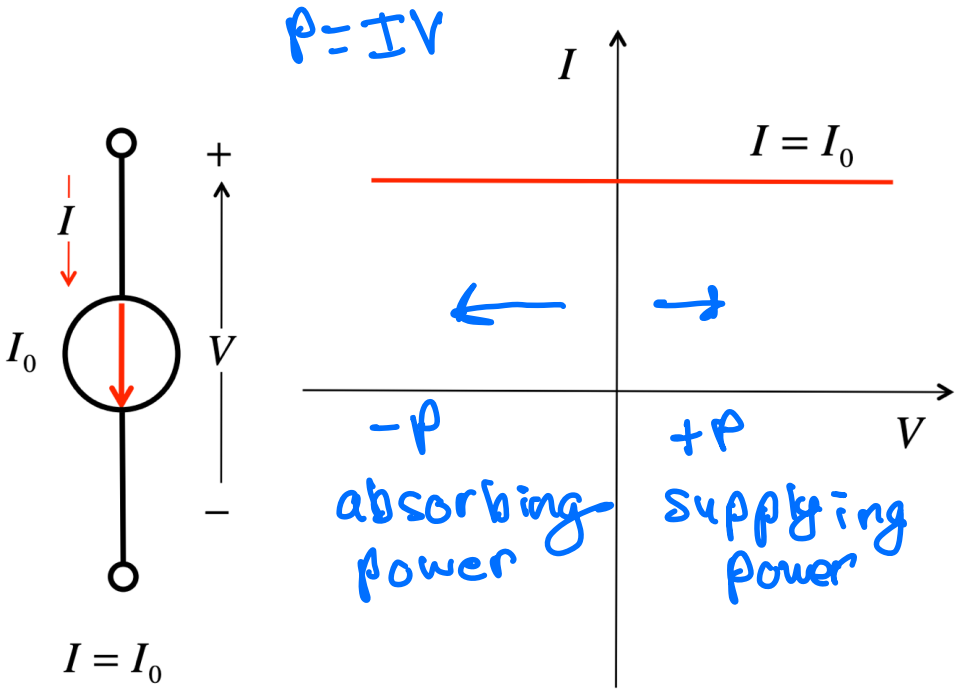
Resistor

Ohm's Law: $I = V/R$ ← constant resistance



Ideal Current Source

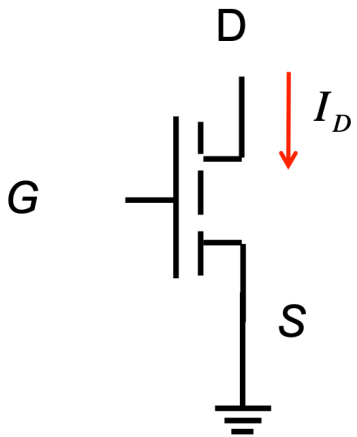
Current flowing from source is constant regardless of the Voltage



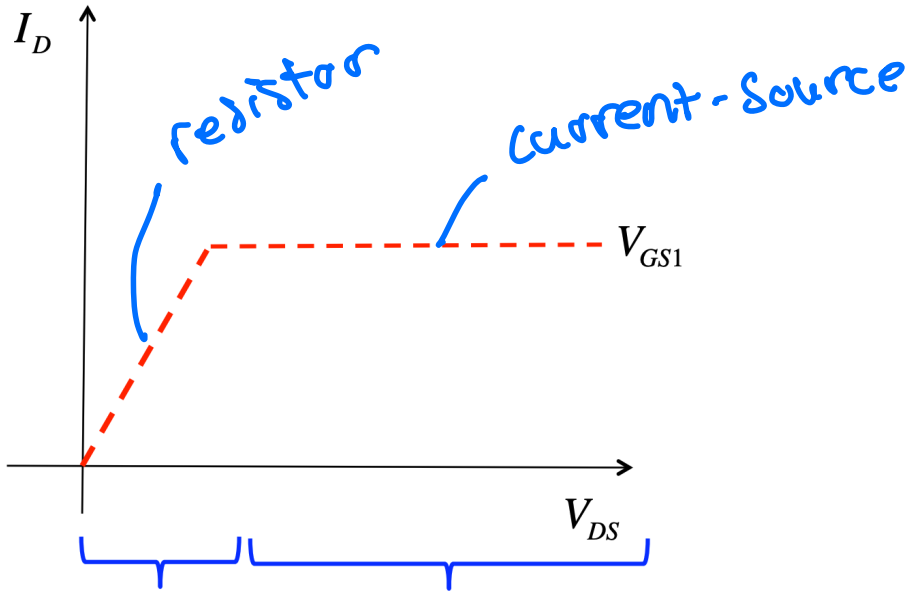
Sources: M. Lundstrom ECE 305 Slides

Ideal I-V Characteristics of a MOSFET

- At low voltages, the device operates as a resistor
- At higher voltages, the device operates like a current source (V_{DS})



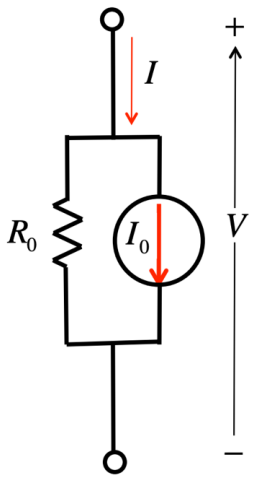
n-channel enhancement mode MOSFET

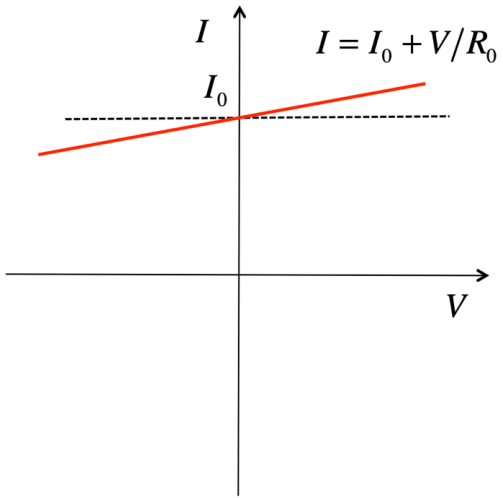


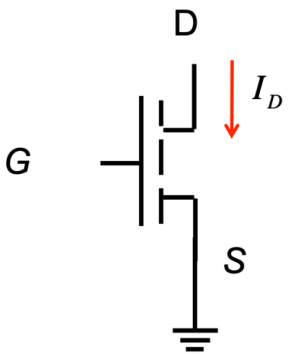
Sources: M. Lundstrom ECE 305 Slides

Realistic I-V Characteristics of a MOSFET

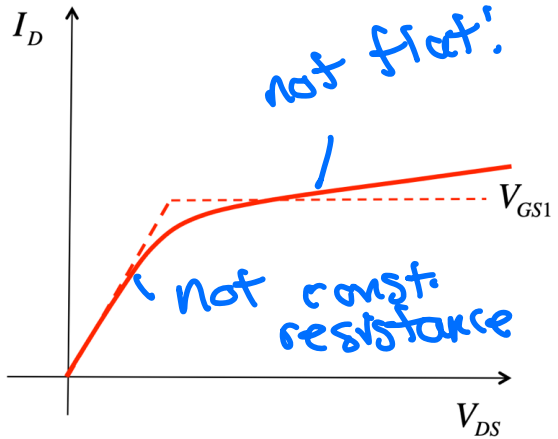
- Real (non-ideal) current sources have an internal source resistance, so the curve is not flat
- The MOSFET also exhibits this non-ideality







n-channel enhancement mode MOSFET



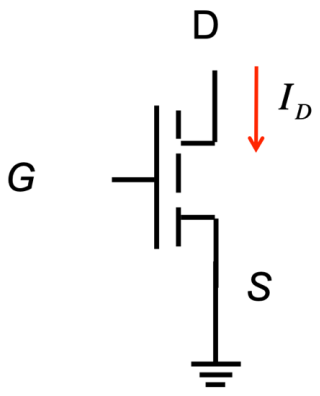
Sources: M. Lundstrom ECE 305 Slides

MOSFET Output Characteristics

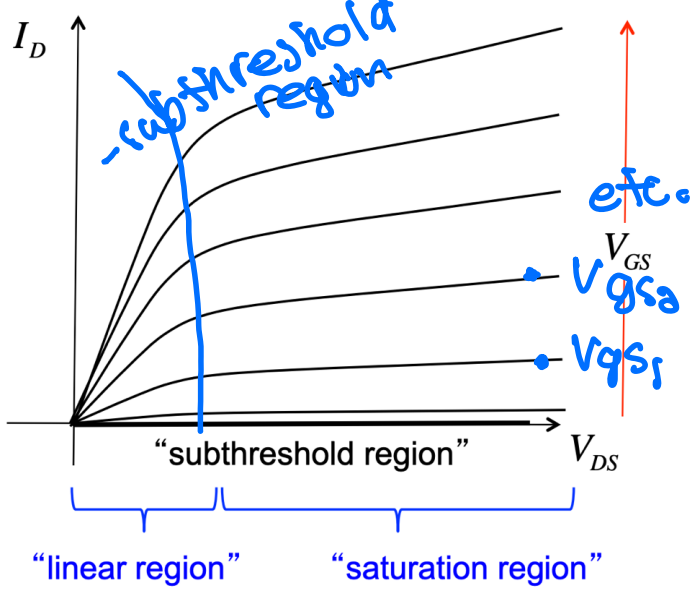
- $I_D - V_{DS}$ sweep where each curve is measured at a fixed V_{GS} value
- Note: Voltages can be denoted by one or two subscripts (e.g. V_g or V_{gs}). Including the "s" for source is essential in complex cases where the source is not necessarily grounded. For our discussions, we will assume the source is grounded and $V_g = V_{gs}$ or $V_d = V_{ds}$

$$V_g = V_{\text{gate}} - V_{\text{ground}}$$

$$V_{gs} = V_g - V_s.$$



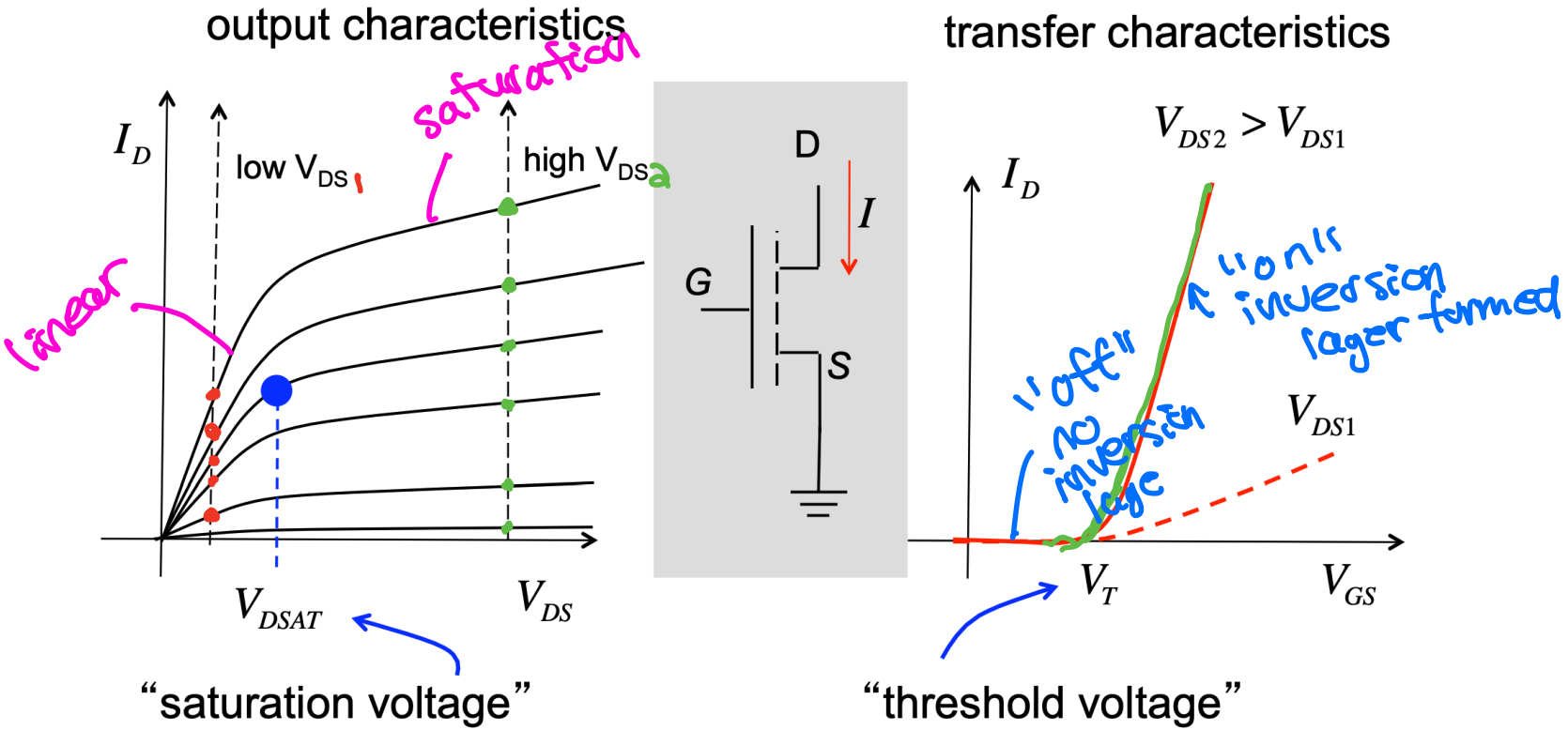
n-channel enhancement mode MOSFET



Sources: M. Lundstrom ECE 305 Slides

MOSFET Transfer Characteristics

- $I_D - V_{GS}$ sweep where each curve is measured at a fixed V_{DS} value



Sources: M. Lundstrom ECE 305 Slides

MOSFET Regions of Operation

1. Cut-off Region: $V_{GS} < V_t$, almost no current flow. Device is "off", switch is open circuit, and the inversion channel is not present or has very low conductivity.
2. Linear (ohmic or triode) Region: : $V_{GS} > V_t$ while $V_{DS} < V_{Dsat}$. The switch is "on" and behaves as a variable resistor (e.g. the resistance is controlled by V_{GS}).
3. Saturation: $V_{GS} > V_t$ while $V_{DS} > V_{Dsat}$ As a higher V_{GS} is applied, the current will reach its maximum and saturate, behaving as a current source controlled by Vgs).

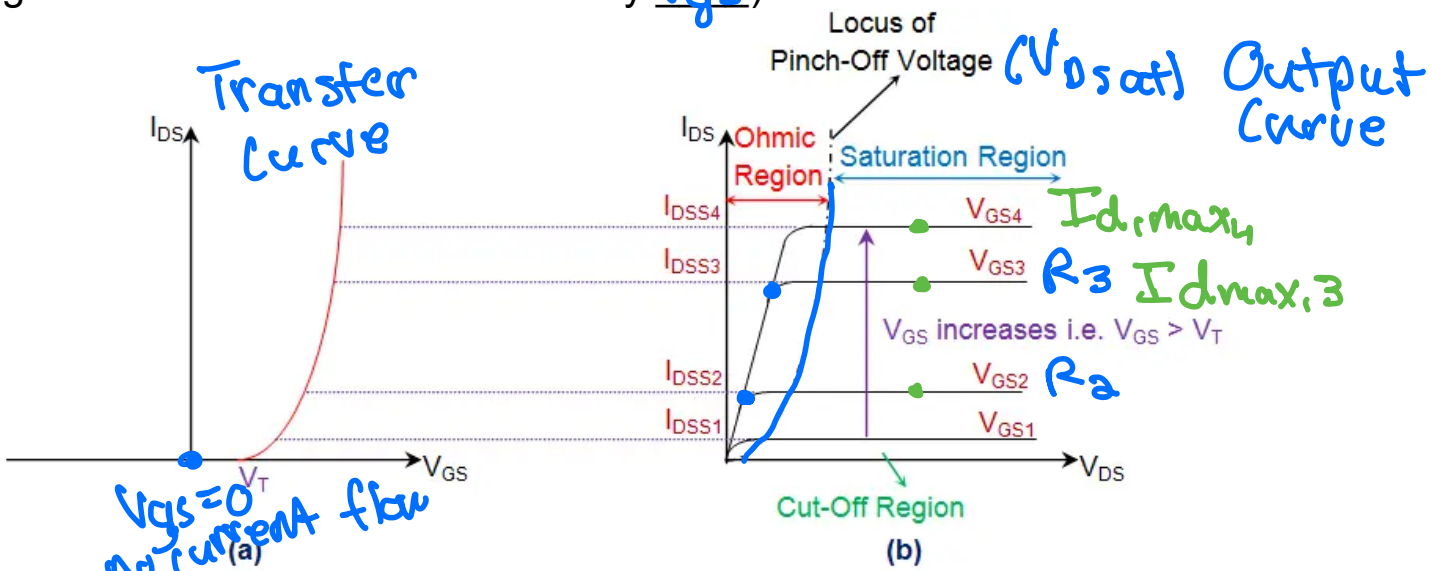


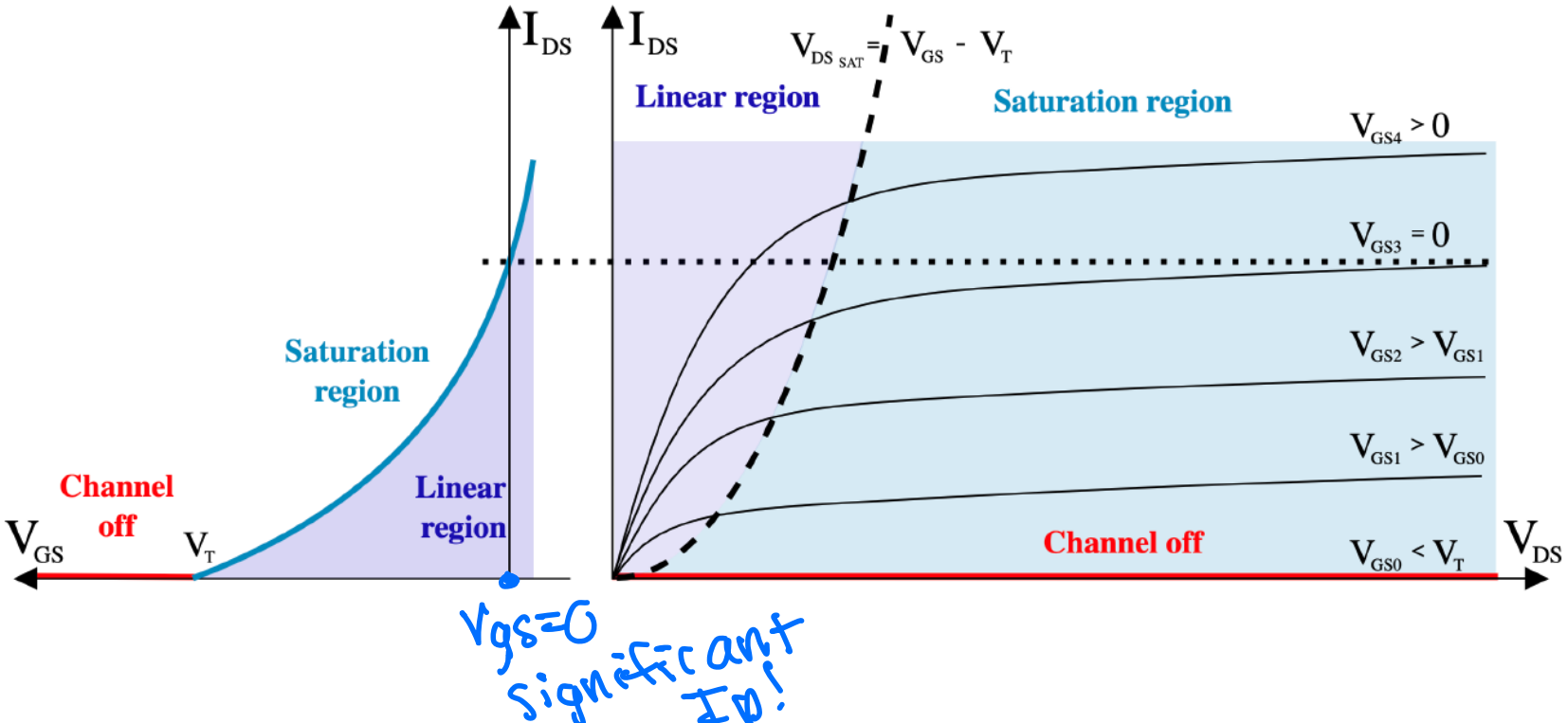
Figure 1 *n*-Channel Enhancement type MOSFET (a) Transfer Characteristics (b) Output Characteristics

Sources: Electrical4U

What about Depletion-Mode I-V?

n-channel

- Depletion-mode FETs have a negative V_{GS} because the channel is present without any applied bias ($V_{GS} = 0$ V)



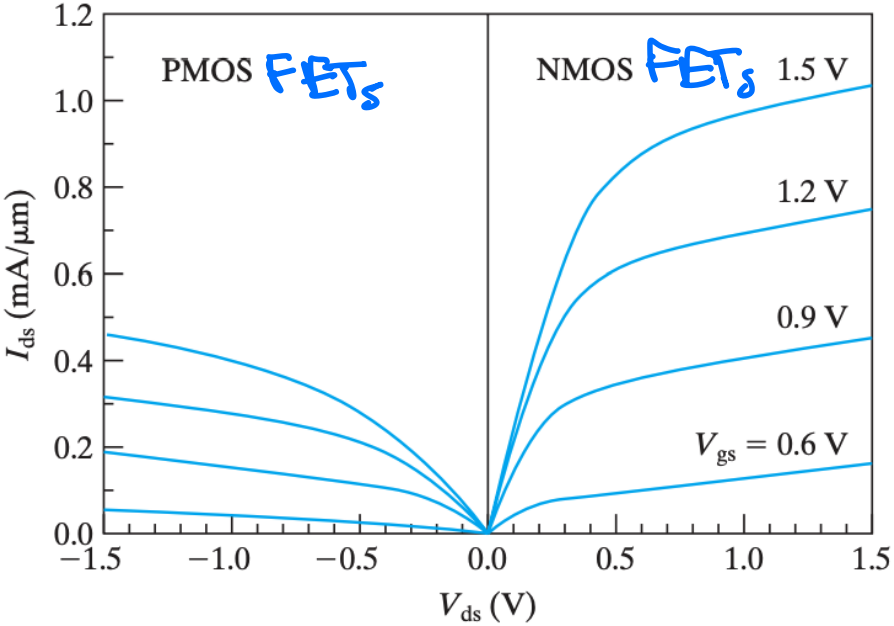
Sources: *Characteristics of depletion-mode FETs, by Phirosiberia – Dispositivos ElectrÅLonicos II - Transistores unipolares ISBN848138630-8., CC BY-SA 4.0.*

What about p-channel MOSFETs?

- The curves are qualitatively similar, but the current is about half as large in the p-channel MOSFET than the n-channel MOSFET. Why?

* Hole mobility less than electron mobility ($\mu_p < \mu_n$)

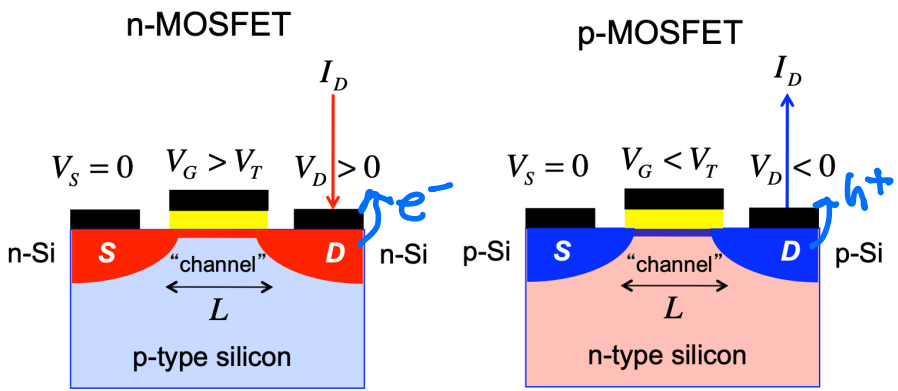
* $v_{sat,p} < v_{sat,n}$



- The polarity of V_{DS} is reversed from that of n-channel MOSFET. Why?

Always denote carriers as flowing source to drain

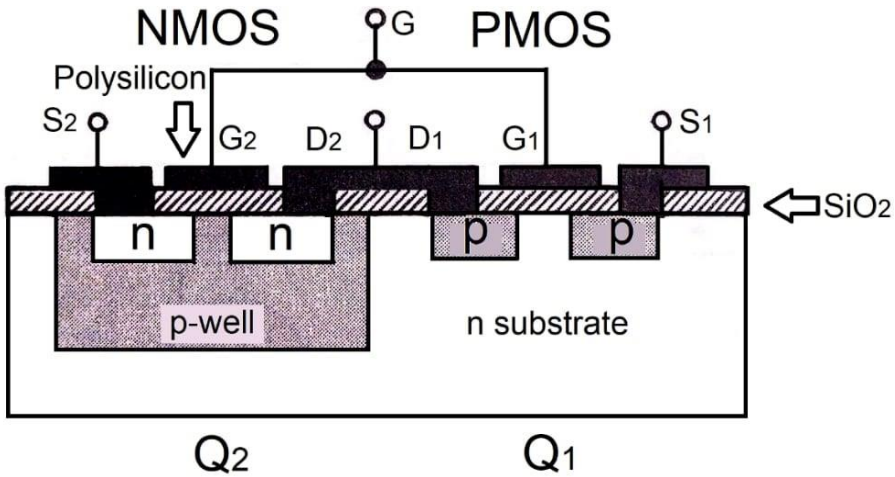
* Id comes into n-MOSFETs, Id comes out p-MOSFETs



Sources: C. Hu *Modern Semiconductor Devices for Integrated Circuits*, M. Lundstrom ECE 305 Slides

CMOS Technology

- Complimentary MOS means the transistors operate in pairs, p-type and n-type on the same chip
- The inversion layer is the conducting channel in a MOSFET.
- Like we learned with MOS capacitors….
  - N-MOSFET or NFET is an N-channel MOSFET
    - Inversion layer is n-type and the substrate is p-type
  - P-MOSFET or PFET is a P-channel MOSFET
    - Inversion layer is p-type and the substrate is n-type
- Primary application is high speed logic gates for digital circuits
- CMOS circuits have negligible DC input current, so the power consumption is low because the "off" transistor limits the drain current to the leakage value
- Power dissipation is notable only during the input switching



Sources: EE Power.com

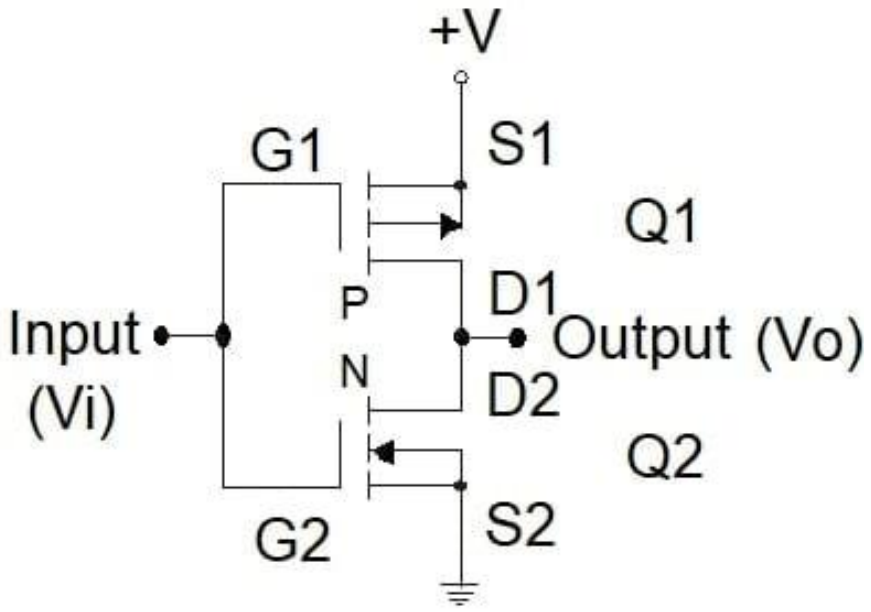
CMOS Inverter Overview

- In binary arithmetic, logic functions are performed with 0 and 1
- Inverter is a logic element that reverses the logic input
- Truth table:

INPUT	OUTPUT
0	1
1	0

- We can build a PMOS or NMOS inverter, but the lowest power dissipation is achieved with CMOS
- Each transistor works as the load resistance of the other

Q1 is an E-mode PMOS
Q2 is an E-mode NMOS



Push-pull configuration:

- Gates are connected at the input
- Drains are connected at the output
- Sources are connected to the respective supply levels (+V and ground)

Sources: EE Power.com

CMOS Inverter: Logic 1 to Logic 0

- What happens when we apply $+V_i$ to the gates? (Logic 1)
- V_{GS2} is (+), and Q2 is turned "on" with $R_{DS,Q2}$ very small
- But $V_{GS1} = 0$ since S1 is also at +V, so Q1 is kept "off" with very high $R_{DS,Q1}$
- The output voltage is computed using the voltage divider rule:

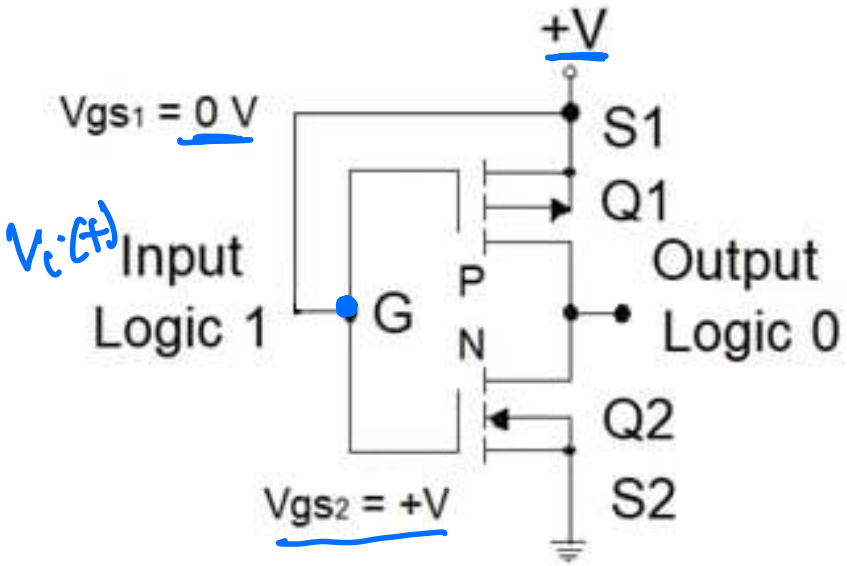
$$V_{out} = V_i \left(\frac{R_{DS,Q2}}{R_{DS,Q1} + R_{DS,Q2}} \right) \approx 0$$

very small

very high

- We have inverted the input Logic 1 to result in an output Logic 0

Q1 is an E-mode PMOS
Q2 is an E-mode NMOS



Sources: EE Power.com

CMOS Inverter: Logic 0 to Logic 1

- Let's look at the opposite case where we connect V_i on the gates to ground (Logic 0)
- $V_{GS2} = 0$, and Q2 is kept "off" with $R_{DS,Q2}$ very high
- Now, $V_{GS1} = -V$ in Q1, and it is "on" with very low $R_{DS,Q1}$
- Once again, we use the voltage divider rule:

$$V_{out} = V_i \left(\frac{R_{DS,Q2}}{R_{DS,Q1} + R_{DS,Q2}} \right) \approx 1$$

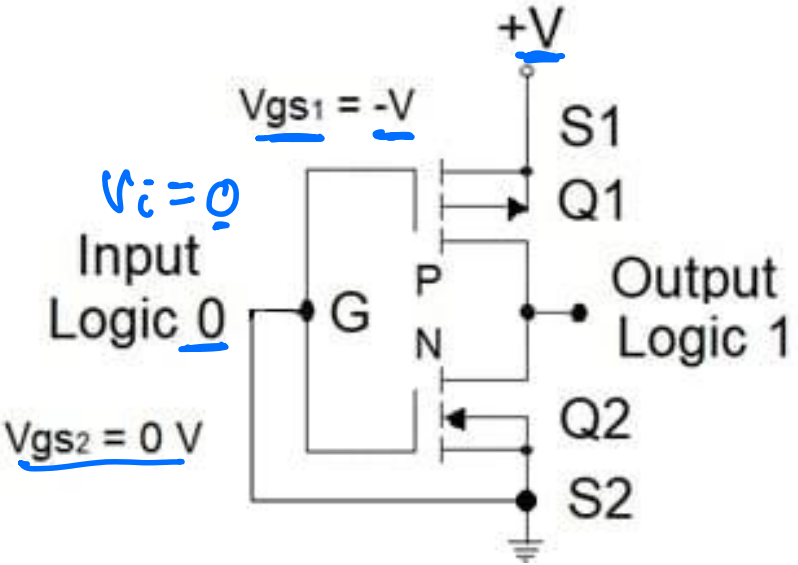
very high

≈ 0

very high

- Thus, we have inverted the input Logic 0 to result in an output Logic 1
- NMOS "pulls-down" output to ground (0) while PMOS "pulls-up" output to +V (1) when "on"

Q1 is an E-mode PMOS
Q2 is an E-mode NMOS



Sources: EE Power.com